UTILITY PATENT APPLICATION TRANSMITTAL
(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	991142	Total Pages	

First Named Inventor or Application Identifier
Junya KAKU

Express Mail Label No.

Check Box if applicable [ ] Duplicate

APPLICATION ELEMENTS FOR:	ADDRESS TO: Assistant Commissioner for Patents
DIGITAL CAMERA	BOX PATENT APPLICATIONS Washington, D.C. 20231

1. [XX] Fee Transmittal Form (Incorporated within this form)
(Submit an original and a duplicate for fee processing)

2. [XX] Specification   Total Pages [15]

3. [XX] Drawing(s) (35 USC 113)   Total Sheets [5]

4. [XX] Oath or Declaration   Total Pages [2]

   a. [XX] Newly executed (original)

   b. [ ] Copy from prior application (37 CFR 1.63(d))
      (for continuation/divisional with Box 17 completed).

      i. [ ] Deletion of Inventor(s)
          Signed statement attached deleting inventor(s) named in prior application,
          see 37 CFR 1.63(d)(2) and 1.33(b).

5. [ ] Incorporation by reference (useable if box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program (Appendix)

7. [ ] Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement Verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [XX] Assignment Papers (cover sheet and document(s))

9. [ ] 37 CFR 3.73(b) Statement (when there is an assignee)   [XX] Power of Attorney

10. [ ] English translation Document (if applicable)

11. [ ] Information Disclosure Statement   [ ] Copies of IDS Citations

12. [ ] Preliminary Amendment

13. [XX] Return Receipt Postcard (MPEP 503)

14. [ ] Small Entity Statement(s)   [ ] Statement filed in prior application
                                                                    Status still proper and desired.

15. [XX] Claim for Convention Priority   [1] Certified copy of Priority Document(s)

    a. Priority of _____ application no. _____ filed on _____ is claimed under 35 USC 119.
       The certified copies/copy have/has been filed in prior application Serial No. _____.
       (For Continuing Applications, if applicable).

16. [ ] Other _____

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

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FEE TRANSMITTAL The filing fee is calculated below	Number Filed	Number Extra	Rate	Basic Fee $760.00
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Independent Claims	1 - 3		x $78.00	
Multiple Dependent Claims			$260.00	
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[XX] A check in the amount of $<u>800.00</u> is enclosed to cover the filing fee of $<u>760.00</u> and the assignment recordation fee of $<u>40.00</u>.

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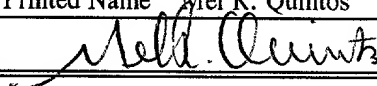
18. CORRESPONDENCE ADDRESS

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TITLE OF THE INVENTION

Digital Camera

BACKGROUND OF THE INVENTION

5   Field of the invention

This invention relates to digital cameras and, more particularly, to a digital camera for displaying subject motion images (through images) real time on the monitor.

Description of the prior art

Where displaying subject through-images having been shot by a digital camera on

10   a built-in monitor, the display image if utilizing an NTSC format requires to be renewed every 1/30 second. Due to this, the shot image data on each frame has to be processed within a brief time, in order to be in time for renewal timing. Meanwhile, the increase in the number of pixels for the CCD imager, in turns, increases the data amount of each frame. Accordingly, process failure might result unless an improvement is contemplated

15   for the processing method.

For this reason, in the conventional digital cameras having pixels in number exceeding one million for example, the pixels to be read out of the CCD imager are subjected to thinning out prior to being outputted for through-images. That is, this includes a process that all the pixels are read out upon depressing the shutter button.

20   However, when outputting a through-image, pixel thinning-out is implemented in order to decrease the amount of data.

However, the conventional method includes switching the pixel read-out scheme between upon outputting through-images and at pressing on the shutter. Consequently, there has been a problem that the CCD imager is complicated in control and hence the

25   circuit therefor becomes complex in configuration.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a novel digital camera which is capable of preventing against process failure.

A digital camera according to the present invention, comprises: an image sensor having a first resolution; a timing generator for reading a first resolution image signal from the image sensor; a first processor for performing predetermined signal processing on the first resolution image signal; a thinning-out circuit for thinning out the first resolution image signal outputted from the first processor and creating a second resolution image signal with a resolution lower than the first resolution; a main memory having at least two memory areas; a selector for selecting alternately the two memory areas; a write controller for writing the second resolution image signal to one of the two memory areas based on an output of the selector; and a read controller for reading a second resolution image signal from the other of the two memory areas based on an output of the selector.

The timing generator reads a first resolution image signal from an image sensor having a first resolution. The first processor performs a predetermined process on the first resolution image signal read from the image sensor. The first resolution image signal outputted from the first processor is thinned out by the thinning-out circuit, being created into a second resolution image signal with a lower resolution than the first resolution. On the other hand, the main memory has at least two memory areas. The selector selects alternately the two memory areas. The write controller writes the second resolution image signal to one of the two memory areas, based on an output of the selector. The read controller reads the second resolution image signal from the other of the two memory areas, based on an output of the same selector.

According to the invention, because the first resolution image signal is thinned out

and created into a second resolution image signal with a low resolution, no failure will be encountered in signal processing even where the CCD imager has an increased resolution. Meanwhile, while writing is being made to one memory area, reading is effected from the other memory area. Accordingly, even where there is difference in operation speed

5   between the areas, the operation on one area will not outpace the operation on the other area. Thus, output images are free from disturbance.

In one aspect of the invention, the timing generator reads out the first resolution image signal in an amount of one screen at an interval of a first predetermined period, and the read controller reading out the second resolution image signal in an amount of one

10   screen at an interval of a second predetermined period shorter than the first predetermined period. In one embodiment of the invention, the second predetermined period is 1/Nth (N is an integer equal to or greater than 2) of the first predetermined period. On another embodiment of the invention, the selector alternately switches for a memory area to be selected at an interval of the first predetermined period.

15   In another aspect of the invention, on a monitor is displayed an image corresponding to an image signal read by the read controller.

In another aspect of the invention, when an instruction key is depressed, a second processor outputs a first disable signal, second disable signal and third disable signal at predetermined timing. The thinning-out circuit is disabled by the first disable signal

20   simultaneously with the operation of the instruction key. The read controller also is disabled by the second disable signal simultaneously with the operation of the instruction key. On the other hand, the write controller writes the first resolution image signal outputted from the first processor to the main memory and disabled by the third disable signal after the first resolution image signal in an amount of one screen has been written.

25   In one embodiment of the invention, a recorder records the first resolution image

signal written on the main memory to a recording medium. The second processor cancels the second disable signal from outputting after the first resolution image signal has been recorded. As a result, the read controller reading the first resolution image signal from the main memory.

5   The above described objects and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

10   Figure 1 is a block diagram showing one embodiment of the present invention;

Figure 2 is a block diagram showing one part of the Figure 1 embodiment;

Figure 3 is an illustrative view showing one SDRAM;

Figure 4 is a flowchart showing one part of operation in the Figure 1 embodiment; and

15   Figure 5 is a flowchart showing another part of operation of the Figure 1 embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figure 1, a digital camera 10 of this embodiment includes a CCD

20   imager 12. The CCD imager 12 has a not-shown color filter mounted at a front thereof. An image of a subject is given to the CCD imager 12 through the color filter.

If an operator operates a mode set switch 56 to a side of camera, a system controller 52 sets for a camera mode. At this time, the CPU 46 starts a signal generator (SG) 16 so that the signal generator (SG) 16 can output a horizontal synchronizing signal

25   and a vertical synchronizing signal. Based on the output horizontal and vertical

synchronizing signals, a TG 14 creates a timing signal to drive the CCD imager 12 by a progressive scan scheme. The CCD imager 12 has vertical lines in number of "1024" and horizontal pixels in number of "768", so that a camera signal (high resolution camera signal) can be outputted with a resolution of XGA. Incidentally, it takes 1/15 second to

5   output a camera signal for each frame.

The output camera signal from the CCD imager 12 is a signal that each pixel has any one of color components. The camera signal thus configured is subjected to well-known noise removal and level adjustment by a CDS/AGC circuit 18, and then converted into camera data as a digital signal by an A/D converter 20. A signal processing circuit 22

10   performs YUV conversion with a ratio of 4:2:2 on the camera data outputted from the A/D converter, thus creating YUV data (high resolution YUV data).

To display real-time motion images (through images) of a subject on a monitor 44, a switch SW1 is connected to a side of a thinning-out circuit 24. That is, the thinning-out circuit 24 is enabled during outputting through-images. The output high-resolution YUV

15   data from the A/D converter 20 is thinned out by the thinning-out circuit, thereby converted into YUV data (low resolution YUV data) having vertical lines in number of "768" and horizontal pixels in number of "480". It should be noted that the pixel data constituting the low resolution YUV data is intermittently outputted without putting close together the pixel data correspondingly to thinning-out.

20   The low resolution YUV data outputted from the thinning-out circuit 24 is sent to a buffer 26a via the switch SW1. The buffer 26a is configured by a dual port SRAM having a capacity corresponding to 128-pixels YUV data. The low resolution YUV data is consecutively written onto the buffer 26a by a buffer write circuit 22a provided in the signal processing circuit 22. That is, the pixel data is put close together in order to

25   eliminate missing portions incurred due to thinning out. This process provides the pixels

with an equivalent pitch to that of pixels of before the thinning-out operation.

The YUV data written on the buffer 26a is read out by a memory control circuit 30 before overwritten by the succeeding YUV data. The memory control circuit fetches the read YUV data through a bus 28, and thereafter writes it to an SDRAM 38 through a bus 36. The clock rate to read data from the buffer 26a is set 4 times a clock rate to write data to the buffer 26a. The buses 28 and 36 are occupied to transfer YUV data from the buffer 26a to the SDRAM 38 in a duration of a quarter of the total period.

Explanation will be concretely made on write operation to the SDRAM 38 with reference to Figure 2. A read request generating circuit 22b included in the signal processing circuit 22 generates a read request at predetermined timing. A write request generating circuit 42b included in an NTSC encoder 42 also generates a write request at predetermined timing. During outputting through-images, the CPU 46 sends a high level gate signal to AND circuits 22c and 42c. This opens the gate to thereby input read and write requests to a mediation circuit 30a. The mediation circuit 30a mediates between the requests, and outputs a predetermined start signal to the processing circuit 30b in order to respond to any of the requests.

To process for a read request from the signal processing circuit 22b, the buffer control circuit 32a sends an address signal to the buffer 26a in response to the start signal and reads YUV data out of the buffer 26a. The read YUV data is fetched into the processing circuit 30b via a bus 28. An SDRAM write circuit 34a writes the fetched YUV data onto the SDRAM 38 through the bus 36. Because the occupation over the buses 28 and 36 at all times excludes other of processing, the processing circuit 30b outputs an end signal to the mediation circuit 30a each time 64-pixels YUV data has been written, thereby opening over buses 28 and 36. Then the mediation circuit 30a enters a next requests process. In this manner, the read requests sent from signal processing

circuit 22 are processed in a plurality of number of times, thereby writing 1-frame low resolution YUV data onto the SDRAM 38 in 1/15 second.

When processing a write request from the NTSC encoder 42, the mediation circuit 30a outputs a predetermined start signal to the processing circuit 30b in response to a write request input. An SDRAM read circuit 34b, in turn, reads YUV data out of the SDRAM 38. Also, a buffer control circuit 32b writes the YUV data read by the SDRAM 38 onto the buffer 26b. The processing circuit 30b generates an end signal when 64-pixels YUV data have been read out, similarly to the above. This puts the buses 28 and 36 open. This operation is repeatedly done, whereby 1-frame low resolution YUV data is read out of the SDRAM 38 in 1/30 second. Incidentally, the buffer 26b is also configured by a dual port SRAM having a capacity to store 128 pixels of YUV data.

The SDRAM 38 includes a bank A and bank B, as shown in Figure 3. A bank switch circuit 40 outputs a bank switch pulse having a level varying every 1/15 second, based on vertical and horizontal synchronizing signal outputted from the SG 16. The SDRAM write circuit 34a assigns a write destination as a bank A when the bank switch pulse is in a high level, and as a bank B when the bank switch pulse is in a low level. On the other hand, the SDRAM reads circuit 34b assign a read destination as a bank B when the bank switch pulse is in a high level, and as a bank A when the bank switch pulse is in a low level. That is, the write and read operations to and from the SDRAM 38 are complementarily done wherein, when one bank is being written by data, the other bank is read of data.

As described above, it takes 1/15 second to write 1 frame of YUV data whereas 1-frame YUV data is completely read out in 1/30 second. Also, the level of a bank switch pulse is changed at an interval of 1/15 second. Due to this, while the YUV data of a current frame is written to one bank, the YUV data of the preceding frame is repeatedly

read out twice. In this manner, there is difference between a time period required for writing and a time period required for reading. Accordingly, if there is provided only one bank, read scanning will outpace write scanning. This results in appearance of a horizontal line on the monitor 44. In order to eliminate such a problem, this embodiment

5   provides the SDRAM 38 with two banks so that write and read operations to and from the banks can be made in a complementary manner.

The buffer read circuit 42a provided in the NTSC encoder 42 reads YUV data stored in the buffer 26b at a quarter rate of a clock of writing. Furthermore, the read YUV data is encoded by an NTSC format. The encoded data is converted by a D/A converter

10   (not shown) into an analog signal to be outputted onto the monitor 44. As a result, through-images are displayed on the monitor 44.

In this manner, when outputting through-images, thinning out is performed on high resolution YUV data to be created every 1/15 second. Thus, YUV data with a decreased resolution down to as low as nearly VGA is outputted from the thinning-out

15   circuit 24 every 1/15 second. That is, the number of pixels is decreased, the pitch of pixels is increased at thinned-out portions, and the data amount per unit time is decreased. The data amount per unit time is decreased at every portion of the image, with a result that no process failure will be encountered in the course of intermittently writing the data onto the SDRAM 38.

20   Meanwhile, because the CCD imager 12 outputs camera signals only every 1/15 second, the duration that the buses 28 and 36 are occupied by transfer of the low resolution YUV data to the SDRAM 38 is reduced down to a half of the conventional. That is, conventionally the camera signals produced every 1/30 second by the CCD imager have been decreased in resolution when outputted from the CCD imager. Due to

25   this, the low resolution YUV data of each frame must have been written to the SDRAM

- 8 -

38 within 1/30 second. Contrary to this, in this embodiment the occupation ratio over the buses 28 and 36 can be reduced to a half of the conventional because the low resolution YUV data of each frame may be written within 1/15 second.

However, the low resolution YUV data must be completely read out of the SDRAM 38 within 1/30 second. Accordingly, the occupation ratio over the buses 28 and 36 during reading is twice a ratio of writing. In other words, the reading from SDRAM 38 is at a twice rate of a rate of writing to the SDRAM 38. To realize this, the present embodiment provides two banks in the SDRAM 38 so that the bank to be written and the bank to be read are switched between in a complementary manner. Thus, the through-image displayed on the monitor 44 is prevented from being deteriorated in image quality.

If the operator operates the shutter button 54, the CPU 46 connects the switch SW1 to the signal processing circuit 22. Also, the gate signal to the AND circuit 42c shown in Figure 2 is decreased to a low level to apply gating to a write request. This disables the thinning-out circuit 24, the SDRAM read circuit 34b and the buffer control circuit 32b. The high resolution YUV data outputted from the signal processing circuit 22 is written to the buffer 26a without being processed of thinning-out. This high resolution YUV data is read out of the buffer 26a by the buffer control circuit 32a each time a read request is outputted from the signal processing circuit 22, and written to the SDRAM 34 by the SDRAM control circuit 34a. In also this case, the bank to be written is determined according to a bank switch signal. Incidentally, the banks A, B each possesses a capacity that can afford to store 1-frame high resolution YUV data. When low resolution YUV data is processed, the bank is utilized at a part thereof.

The high resolution YUV data is greater in the number of pixels than the low resolution YUV data, hence requiring a correspondingly longer time in being written onto the SDRAM 38. However, the occupation ratio over buses 28 and 36 is decreased

correspondingly to suspension of data reading from the SDRAM 38. This reduction of occupation ratio is allocated to data writing onto the SDRAM 38. Consequently, there is no possibility that process failure occurs during writing the high resolution YUV data onto the SDRAM 38.

When the high resolution YUV data has been completely written to the SDRAM 38, i.e., when elapsing 1/15 second from depressing the shutter button 54, the CPU 46 also reduces to a low level the gate signal to be supplied to the AND circuit 22c shown in Figure 2. This applies gating also to the read request, thus suspending the writing to the SDRAM 38.

Incidentally, the switch SW2 is connected to a black image generating circuit 41 in response to operation of the shutter button 54. This supplies black image data to the NTSC encoder 42. Thus, a black image is displayed on the monitor 44 simultaneously with pressing on the shutter.

The 1-frame high resolution YUV data stored within the SDRAM 38 is delivered to the JPEG CODEC 45 where it is subjected to JPEG compression. The resulting compression data is once written to the SDRAM 38, and thereafter recorded onto a memory card 50. After completing the recording, the switch SW2 is returned and further the gate signal to be supplied to the AND circuit 42c is returned to the high level. Due to this, the high resolution YUV data stored within the SDRAM 38 is read out, and the display on the monitor 44 is turned from the black image to a freeze image. When the freeze image is displayed, the SDRAM 38 is kept suspended from being written on, providing a corresponding amount of vacancy to the buses 28 and 36. Accordingly, no process failure will occur in the buffer 26 despite the number of pixels of the high resolution YUV data is greater than that of the low resolution YUV data.

Incidentally, the monitor 44 has a resolution that is lower than any of the high

resolution YUV data and the low resolution YUV data. Consequently, the NTSC encoder 42 performs thinning-out on the high resolution YUV data and low resolution YUV data in conformity to their number of pixels.

The CPU 46 processes concretely a flowchart shown in Figure 4 and Figure 5. First, in step S1 DMA is started for a camera signal process block. That is, the SG 16 is started, and the switch SW1 is connected to the thinning-out circuit 24 and a high level gate signal is supplied to the signal processing circuit 22. The signal processing circuit 22 writes low resolution YUV data onto the buffer 26a and sends a read request to the memory control circuit 30. As a result, the low resolution YUV data is written to the SDRAM 38. Then, the CPU 46 in step S3 starts DMA for an encode block. That is, a high level gate signal is delivered to the NTSC encoder 42. Due to this, a write request is sent to the memory control circuit 30, and the low resolution YUV data read out of the SDRAM 38 is written to the buffer 26b. The NTSC encoder 42 further processes the low resolution YUV data written on the buffer 26b. As a result, through-images are displayed on the monitor 44.

If the shutter button 54 is operated by the operator, the CPU 46 in step S5 determines "YES". Then, in step S7 the switches SW1 and SW2 are respectively connected to the signal processing circuit 22 and the black image generating circuit 41. In step S9 a gate signal to be supplied to the NTSC encoder 42 is reduced to a low level. Accordingly, the high resolution YUV data is written to the SDRAM 38 whereby a black image is displayed on the monitor 44. In step S11 it is determined whether 1/15 second has been elapsed from depressing the shutter button 54 or not. If "YES", then in step S13 a gate signal to be supplied to the signal processing circuit 22 is lowered from a high level to a low level. Due to this, the writing to the SDRAM 38 is suspended.

Subsequently, in step S15 the high resolution YUV data is recorded. If the

recording process has been completed, then in step S17 "YES" is determined. In respective steps of S19 and S21, the switch SW2 is returned and the gate signal to be supplied to the NTSC encoder 42 is returned to the high level. Accordingly, a freeze image is displayed in place of the black image on the monitor 44. In step S23 it is

5   determined whether a predetermined time has elapsed from the operation of the shutter button 54 or not. If "YES", then in step S25 the switch SW1 is returned. In step S27 the gate signal to be supplied to the signal processing circuit 22 is returned in level. Then the process returns to the step S5. As a result, through-images are displayed again on the monitor 44.

10   Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

WHAT IS CLAIMED IS:

1. A digital camera, comprising:

an image sensor having a first resolution;

a timing generator for reading a first resolution image signal from said image

sensor;

a first processor for performing predetermined signal processing on said first

resolution image signal;

a thinning-out circuit for thinning out said first resolution image signal outputted

from said first processor and creating a second resolution image signal with a resolution

lower than said first resolution;

a main memory having at least two memory areas;

a selector for selecting alternately said two memory areas;

a write controller for writing said second resolution image signal to one of said

two memory areas based on an output of said selector; and

a read controller for reading a second resolution image signal from the other of

said two memory areas based on an output of said selector.

2. A digital camera according to claim 1, wherein said timing generator reads out

said first resolution image signal in an amount of one screen at an interval of a first

predetermined period, and said read controller reading out said second resolution image

signal in an amount of one screen at an interval of a second predetermined period shorter

than said first predetermined period.

3. A digital camera according to claim 2, wherein said second predetermined

period is 1/Nth (N is an integer equal to or greater than 2) of said first predetermined

period.

4. A digital camera according to claim 2, wherein said selector alternately

switches for a memory area to be selected at an interval of said first predetermined period.

5. A digital camera according to claim 1, further comprising a monitor to display an image corresponding to an image signal read by said read controller.

6. A digital camera according to claim 1, further comprising:

an instruction key; and

a second processor for outputting at predetermined timing a first disable signal, a second disable signal and a third disable signal in response to operation of said instruction key; wherein

said thinning-out circuit being disabled by said first disable signal simultaneously with the operation of said instruction key,

said read controller being disabled by said second disable signal simultaneously with the operation of said instruction key, and

said write controller writing said first resolution image signal outputted from said first processor to said main memory and disabled by said third disable signal after said first resolution image signal in an amount of one screen has been written.

7. A digital camera according to claim 6, further comprising a recorder to record said first resolution image signal written on said main memory to a recording medium.

8. A digital camera according to claim 7, wherein said second processor cancels said second disable signal from outputting after said first resolution image signal has been recorded, and said read controller reading said first resolution image signal from said main memory.

9. A digital camera according to claim 1, wherein said memory has a single signal input/output port.

ABSTRACT OF THE DISCLOSURE

A digital camera includes a monitor. When outputting through-images on the monitor, high-resolution YUV data outputted from a signal processing circuit is thinned out and created into low-resolution YUV data. The low resolution YUV data of a current frame is written to one of banks formed within an SDRAM in 1/15 second. On the other hand, the low resolution YUV data of the preceding frame is read out of the other bank in 1/30 second. That is, reading is made twice within 1/15 second. The low resolution YUV data thus read is thereafter processed by an NTSC encoder and outputted onto the monitor.

FIG. 1

10

12   18 CDS/AGC   20 A/D   22 SIGNAL PROCESSING   22a   24 THINNING OUT   SW1   26a BUFFER

16 S G   14 T G   40 BANK SWITCH

38 SDRAM   36   30 MEMORY CONTROL

41 BLACK IMAGE GENERATION   SW2   26b BUFFER   26c   42 NTSC ENCODER   42a   44 MONITOR

45 JPEG CODEC   26c BUFFER   28

52 SYSTEM CONTROLLER   CONTROL SIGNAL   54 SHUTTER BUTTON   56 MODE CHANGE SWITCH

50 MEMORY CARD   46 C P U

FIG. 2

FIG. 3

<u>38</u>

BANK A
BANK B

FIG. 4

```
            ┌─────────────────────┐
            │     CAMERA MODE     │
            └─────────────────────┘
                      │
                      ▼
        ┌───────────────────────────┐
   S1 ──│ START DMA FOR CAMERA      │
        │ SIGNAL PROCESS BLOCK      │
        └───────────────────────────┘
                      │
                      ▼
        ┌───────────────────────────┐
   S3 ──│ START DMA FOR             │
        │ ENCODE BLOCK              │
        └───────────────────────────┘
                      │
    (B)───────────────┼
                      ▼
   S5          ◇─────────────◇       NO
              │  SHUTTER ON   │─────────
               ◇      ?      ◇
                      │ YES
                      ▼
        ┌───────────────────────────┐
   S7 ──│ OPERATE SWITCH            │
        │ SW1, SW2                  │
        └───────────────────────────┘
                      │
                      ▼
        ┌───────────────────────────┐
   S9 ──│ SUSPEND READING FROM      │
        │ SDRAM                     │
        └───────────────────────────┘
                      │
                      ▼
   S11         ◇──────────────◇      NO
              │ 1 / 15 SECOND │─────────
              │   ELAPSED     │
               ◇     ?      ◇
                      │ YES
                      ▼
        ┌───────────────────────────┐
   S13──│ SUSPEND WRITING TO        │
        │ SDRAM                     │
        └───────────────────────────┘
                      │
                      ▼
        ┌───────────────────────────┐
   S15──│   RECORD PROCESS          │
        └───────────────────────────┘
                      │
                      ▼
                    (A)
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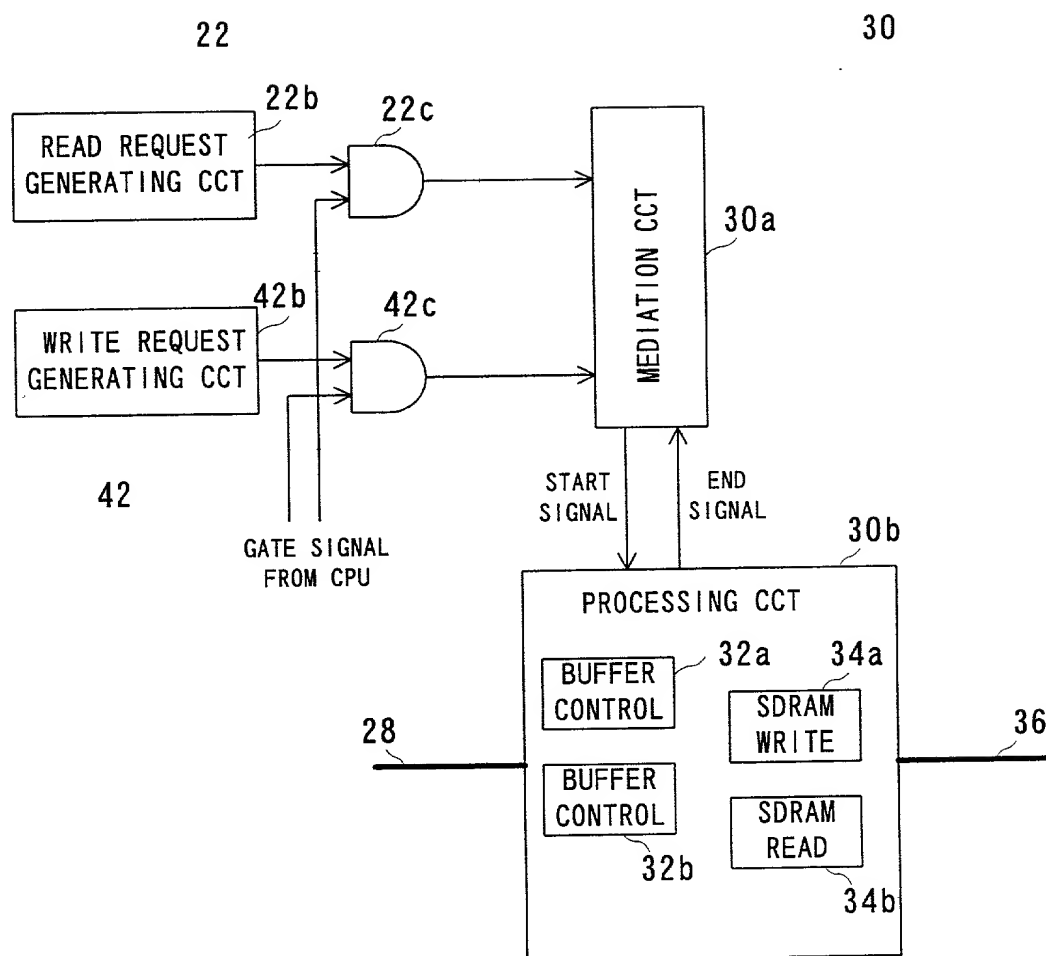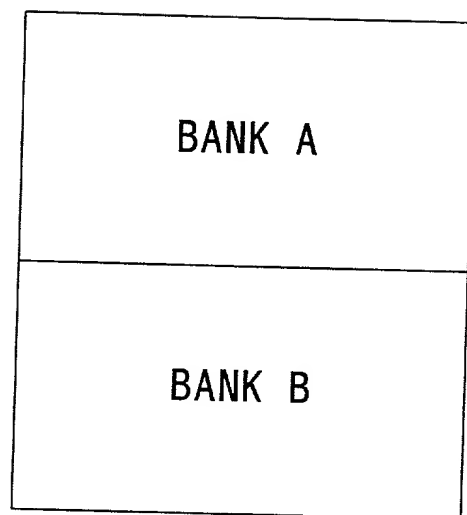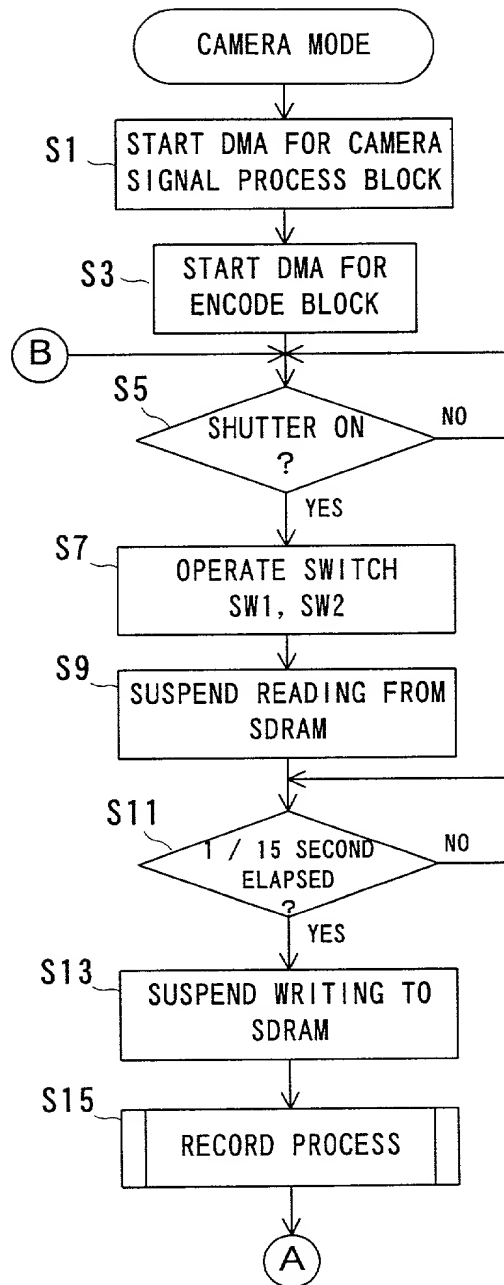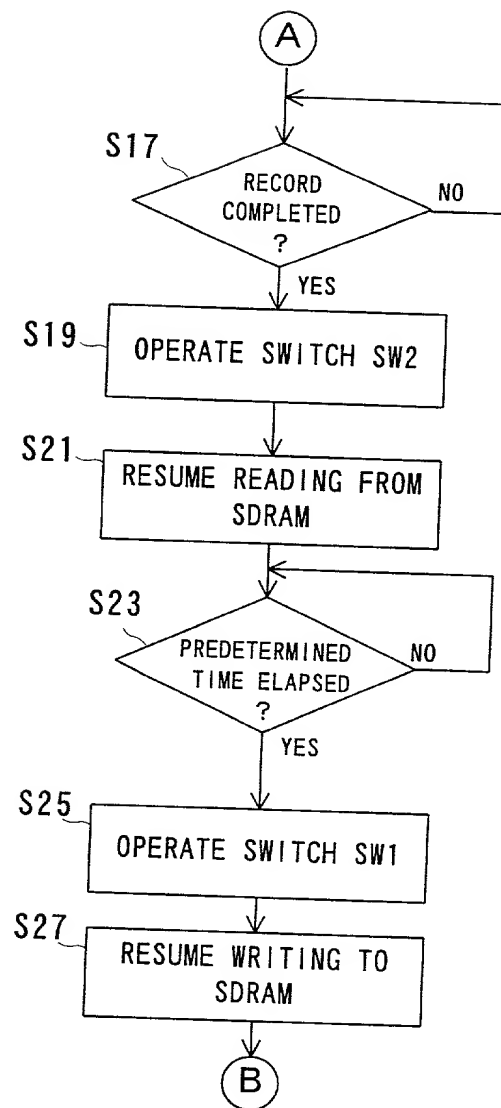
FIG. 5

Declaration For U.S. Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention **entitled** (Insert Title) _____DIGITAL CAMERA_____

the specification of which is attached hereto unless the following is checked:

☐   was filed on _____as United States Application Number or PCT International

Application Number_____and was amended on _____

(if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a) - (d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

(List prior foreign applications. See note A on back of this page)

Patent Application No. 10-291995	Japan	14 October 1998	Priority Claimed ☒ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)	
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No

(See note B on back of this page)   ☐ See attached list for additional prior foreign applications

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of the application:

(List Prior U.S. Applications)

(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18 of the United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor (given name, family name) __Junya KAKU__

(See note C above)

Inventor's Signature ___Junya Kaku___ Date __September 29, 1999__

Residence __Itami-shi, HYOGO, Japan__ Citizenship __Japanese__

Post Office Address __2-1-11-804, Miyanomae, Itami-shi, HYOGO, Japan__

Full name of second inventor (given name, family name)_____

Inventor's Signature_____Date _____

Residence_____Citizenship _____

Post Office Address _____

Full name of third inventor (given name, family name) _____

Inventor's Signature_____Date _____

Residence_____Citizenship _____

Post Office Address _____

Full name of fourth inventor (given name, family name) _____

Inventor's Signature_____Date _____

Residence_____Citizenship _____

Post Office Address _____

Full name of fifth inventor (given name, family name)_____

Inventor's Signature_____Date _____

Residence_____Citizenship _____

Post Office Address _____

Full name of sixth inventor (given name, family name) _____

Inventor's Signature_____Date _____

Residence_____Citizenship _____

Post Office Address _____

Full name of seventh inventor (given name, family name) _____

Inventor's Signature_____Date _____

Residence_____Citizenship _____

Post Office Address _____

Full name of eighth inventor (given name, family name) _____

Inventor's Signature_____Date _____

Residence_____Citizenship _____

Post Office Address _____